Rejections Under 35 U.S.C.§102

Claims 1, 8, and 11 were rejected under 35 U.S.C.§102(b) as being anticipated by IBM Technical disclosure bulletin (Cross-reference 0018-8689-20-8-3117, hereinafter "'3117"). Claims 1 and 8 have been canceled, and therefore the concerns expressed in the Office Action with respect to these claims are moot. The Applicant respectfully traverses the rejection of claim 11, and will demonstrate how the claim language distinguishes this embodiment of the invention over the cited art in the discussion which follows.

The Office Action asserts that '3117 discloses "a first plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer; a second plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and a third plurality of conductive vias (16) downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer." However, this is not what is claimed by the Applicant. Claim 11 recites:

> a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first *and* third conductive layers (emphasis added)

Therefore, since '3117 does not disclose each of the elements claimed by the Applicant, especially "conductive vias ... to provide electrical interconnection to the first *and* third conductive layers", it is respectfully requested that the rejection of claim 11 under § 102 be reconsidered and withdrawn.

Rejections Under 35 U.S.C.§103

Claims 4-5, 13, 19, and 21 were rejected under 35 U.S.C.§103(a) as being unpatentable over '3117. Claims 2-3 were rejected under 35 U.S.C.§103(a) as being unpatentable over '3117 in view of Herrell (U.S. Patent No. 6,191,479, hereinafter "Herrell"). The Applicant respectfully traverses these rejections of the claims, and will demonstrate how a *prima facie* case of obviousness has not been established in the discussion which follows.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The fact that references can be combined or modified does not render the resultant combination obvious *unless* the prior art *also* suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. That is, unless all three of the conditions described in M.P.E.P. § 2142 are met, a *prima facie* case of obviousness is not established, and rejection under 35 U.S.C.§103 is improper. The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which notes that the motivation must be supported by evidence in the record.

With respect to claims 4, 5, 13, and 21, it is admitted in the Office Action that '3117 does not disclose the material composition of the conductive or insulator layers in a capacitor, as claimed by the Applicant. It is then asserted that "it is well known in the capacitor art to form"

insulating layers from a BaSrTiO3 material, and conductive layers from a copper material. However, no evidence in the record supports this assertion.

Since all of the claimed elements are not found in the '3117 reference, the Applicant assumes that the Examiner is taking official notice of the missing elements. The Applicant respectfully objects to such official notice using a single reference obviousness rejection, and pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

In addition, as noted in a previous response by the Applicant, some references in the art (e.g., Farooq et al., previously cited) teach away from the use of SBT as an insulator, since it is noted that a low-K material can be key to the construction of a capacitor. (e.g., see Farooq et al. col. 5, lines 27-32). References must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. "Obvious to try" is not a proper standard for determining obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir., 1988). "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988). Since no reference is supplied to support these assertions, and since one of the assertions contradicts the teaching of a reference already in the record (i.e., Farooq et al.), it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

With respect to claim 19, it is admitted in the Office Action that '3117 does not disclose vias "extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the ... capacitor." It is then asserted that "it is well known in the capacitor art to "extend vias through a substrate to provide electrical interconnections to both sides of the capacitive element" and that it would be obvious to "extend the vias of '3117 through the substrate to provide electrical interconnections to both sides of the capacitor, since such a modification would decrease the space needed in the electrical system." However, no evidence in the record supports this assertion.

Since all of the claimed elements are not found in the '3117 reference, the Applicant assumes that the Examiner is taking official notice of the missing elements. The Applicant respectfully objects to such official notice using a single reference obviousness rejection, and

pursuant to M.P.E.P. § 2144.03, respectfully traverses the assertion of official notice and respectfully requests that additional references be cited in support of this position.

In addition, it is noted in the '3117 reference that "the tap-off pads 12 of the capacitor are distributed and exactly correspond in location to the voltage supply pads 14 of the chip." Again, as noted previously, references must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. Allowing conductive vias to penetrate the substrate in '3117 does not support an "*exact* correspondence in location to the voltage supply pads of the chip." Since no reference is supplied to support the assertion in the Office Action, and since the assertion contradicts the teaching of the '3117 reference, it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Finally, with respect to claims 2-3, it is admitted in the Office Action admits that '3117 does not disclose controlled collapse chip connection (C4) lands fabricated on the third insulator layer. It is then asserted that Herrell teaches the use of C4 lands and that it would be obvious to "modify the capacitor of '3117 using the C4 lands as taught by Herrell, since such a modification would decrease the space used in the electrical system by placing the capacitor directly onto the chip" and form "multiple C4 lands which is [sic] fabricated in staggered columns in plain view, since such modifications would allow additional connections to the capacitor of '3117."

The Office Action assertion overlooks the statement in the '3117 reference that "the tap-off pads 12 of the capacitor are distributed and exactly correspond in location to the voltage supply pads 14 of the chip," as well as the placement of the chip 20 and capacitor 18 in FIG. 2 of this reference. No need is expressed in the '3117 reference to place the capacitor "directly on the chip" (in fact, such placement would make it impossible to properly mount the chip to the circuit board shown in FIG. 2 of '3117). Thus, there is no motivation to combine the references since '3117 teaches away from the combination of '3117 and Herrell. Further, since no reference is supplied to support the Office Action assertion, it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). Finally, with respect to claim 3, it should be noted that if an independent claim (e.g., amended claim 2) is nonobvious under 35 U.S.C.§ 103, then any claim depending therefrom is nonobvious. See M.P.E.P. § 2143.03

In summary, since the '3117 reference and Herrell do not disclose each and every element of the embodiments of the invention claimed by the Applicant, and since there is no motivation to combine the references, such that a *prima facie* case of obviousness has not been established, it is respectfully requested that the rejection of claims 2-5, 13, 19, and 21 under § 103 be reconsidered and withdrawn.

ALLOWABLE SUBJECT MATTER

The Applicant notes with appreciation that claims 9-10 and 14-18 have been allowed. It is also noted that claims 6-7, 12, and 20 stand objected to as being dependent upon a rejected base claim, but are indicated as allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

CONCLUSION

The Applicant respectfully submits that claims 2-7 and 9-21 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 13 day of January, 2003.

Jane Sagers
Name

Jane Sagers
Signature

Clean Version of Pending Claims

MULTI-LAYER CHIP CAPACITOR
Applicant: Larry Eugene Mosley
Serial No.: 09/537,274

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2. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

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a third insulator layer located over the third conductor layer;

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and

a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, wherein at least one of the conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

5. The multi layer integrated circuit capacitor of claim 4 wherein at least one of the conductive layers are fabricated from a copper.

6. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer;

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and

a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

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a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

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a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

9. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

10. The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

11. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

12. The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

13. The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

14. A circuit board assembly comprising:

a circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit die comprising a capacitor having:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

15. The circuit board assembly of claim 14 wherein the second integrated circuit die comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

18. The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

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a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

20. The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

21. The multi layer integrated circuit capacitor of claim 1 wherein each of the conductor layers comprise a metal material and wherein each of the insulator layers comprise $BaSrTiO_3$.